APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,342	10/21/2003	Shih-Lien L. Lu	42P11877C	6642

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EXAMINER
WALTER, CRAIG E

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 10/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _07 January 2005_.

2a)☐ This action is **FINAL.**   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-23_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-23_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _07 January 2005_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _7/2/04, 10/21/03_.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

Priority

1.   Applicant's claim for the benefit of a prior-filed application under 35 U.S.C. 119(e)

or under 35 U.S.C. 120, 121, or 365(c) is acknowledged.

Information Disclosure Statement

2.   The information disclosure statements (IDS) submitted on 02 July 2004 and 21

October 2003 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the

information disclosure statements have been fully considered by the examiner.

Specification

3.   The disclosure is objected to because of the following informalities:

      The lengthy specification has not been checked to the extent necessary to

determine the presence of all possible minor errors. Applicant's cooperation is

requested in correcting any errors of which applicant may become aware in the

specification.

      Appropriate correction is required.

Double Patenting

4.   Claims 1-23 of the instant application contain every element of claims 1-5, 9-20,

22-24, and 26-28 of application 09/966,586 (filing date 9/28/01) and as such, anticipate

claims 1-23 of the instant application.

"A later patent claim is not patentably distinct from an earlier patent claim

if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi,

759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type

double patenting because the claims at issue were obvious over claims in four

prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir.

1998) (affirming a holding of obviousness-type double patenting where a patent

application claim to a genus is anticipated by a patent claim to a species within

that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC.,

United States Court of Appeals for the Federal Circuit, ON PETITION FOR

REHEARING EN BANC (DECIDED: May 30, 2001).

As for claim 1, every element in the instant applicant is present in

application 09/966,586 as shown below:

Claim 1: Application 09/966,586 (US PG Publication - 2003/0065884)	Claim 1: Instant Application
An apparatus comprising: a cache to provide access to contents of a memory bank;	An apparatus comprising: a cache to provide access to contents of a memory bank;
more than two global buses to provide parallel access to said cache and the memory bank;	more than two global buses to provide parallel access to said cache and the memory bank;
and a cache controller to maintain a content of the memory	and a cache controller to maintain a content of the memory
bank in said cache via parallel access of said cache and the memory bank	bank in said cache via parallel access of said cache and the memory bank
to respond to a request for an access of the memory bank substantially independent of a latency to refresh the memory bank.	to respond to a request for an access of the memory bank substantially independent of a latency to refresh the memory bank.

Claim 2, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22,

and 23 of the instant application correspond to claims 2, 4, 5, 17, 10, 11, 12, 13, 14, 15,

16, 17,18,19, 20, 22, 23, 24, 26, 27 and 28 of application 09/966,586 respectively.

Further, claim 3 of the instant application is merely a combination of

claims 3 and 9 of application 09/966,586 therefore it too is anticipated (as 3 and 9 of

application 09/966,586 both depend on claim 1).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly
claiming the subject matter which the applicant regards as his invention.

5.   Claims 1-23 are rejected under 35 U.S.C. 112, second paragraph, as being

indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention.

As for claim 1, 7, 9, 16, 19 and 21, the phrase "substantially independent"

as in claim 1; "substantially simultaneous" as in claim 7; "substantially in parallel"

as in claim 9; "substantially independent" as in claim 19; and "substantially in

parallel" as in claim 21, renders the claims indefinite as the specification fails to

provide any standard for ascertaining the requisite degree to which the term

"substantially" limits the scope of the claimed invention. The claims will further

be treated on their merits based on the assumption that "substantially

simultaneous" is taken to mean two or more events that occur simultaneously;

"substantially independent" is to mean "independent"; and "substantially in

parallel" is to mean "in parallel".

Claims 2-6, 8, 10-15, 17-18, 20, and 22-23 are further rejected as they too

inherit all the claim limitations of one of each of the five aforementioned rejected

claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6.   Claims 9-15, and 21-23 are rejected under 35 U.S.C. 102(b) as being anticipated

by Leung et al., hereinafter Leung (US Patent 5,999,474).

As for claims 9 and 21, Leung teaches a method (and medium in claim

21), comprising:

receiving a request for an access for contents of a memory bank

(col. 3, lines 20-28 – during read access data is read from the bank);

maintaining a content of the memory bank in a cache (col. 3, lines 20-28 – data is

written to a cache);

accessing the contents of the memory bank and the cache

substantially in parallel in response to said maintaining (col. 3, lines 20-28 – access to

the bank and cache is provided via the data bus simultaneously) and to respond to the

request substantially independent of a latency to refresh the memory bank. (Col. 2,

lines 34-37, Leung teaches memory banks in parallel with a buffer, each bank

independently controlled such that refresh operations of the banks can be controlled

independently. Leung further discloses performing the refresh operating without

delaying external access to the device in lines 63-65 of col. 2. Additionally Leung

teaches the refresh operation as occurring within the banks when a cache hit occurs –

col. 3, lines 7-11).

As for claim 10, Leung teaches the method of claim 9, wherein said

receiving comprises receiving a request for an access for the memory bank when a

refresh is pending (referring to Fig. 4, during time period T5, a refresh request is

pending and detected. At this same time a read transaction request is detected – col.

13, lines 26-30). Leung further teaches only refreshing when no bank access is

pending – col. 4, lines 25-27. In other words when a request is received during a

pending refresh operation, the refresh will not occur until the bank access is completed.

As for claims 11 and 22, Leung teaches the method of claim 9 (and

medium of claim 22), wherein said maintaining comprises:

direct mapping a line of the memory bank into the cache (col. 2,

lines 55-60 – cache is of direct map configuration); and

storing a tag associated with the line of the memory bank (Fig. 2,

element 185 – the cache tag stores addresses of the memory bank – col. 6, lines 5-

10).

As for claim 12, Leung teaches the method of claim 9, wherein said maintaining comprises determining a refresh conflicts with the access (col. 3, lines 3-12, memory banks are not accessed when cache hit occurs (however the cache is now being accessed). Once this is determined the pending refresh operation is performed within the banks).

As for claims 13, 14 and 23, Leung teaches the method of claim 9 (and medium of claim 23), wherein said accessing comprises reading from (and writing to) the memory bank substantially simultaneously with reading from (writing to) the cache (col. 3, lines 20-28 – access (reading or writing) to the bank and cache is provided via the data bus simultaneously).

As for claim 15, Leung teaches the method of claim 9, wherein said accessing comprises:

turning off read access to the cache for a first global bus during a cycle and turning on write access to the cache for a second global bus during the cycle after turning off read access (Fig. 1 depicts dedicated read and write global buses DB and DA respectively. Further if a cache miss occurs (i.e. read operation determines that the requested data is not present), the read operation completes and a write operation is initiated in order write back to the cache – col. 3, lines 40-45).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7.   Claims 1-8 and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saulsbury et al., hereinafter Saulsbury (US Patent 6,199,142 B1) as applied to claim 9 (and claim 21) above, and in further view of Leung.

As for claim 1, Saulsbury teaches an apparatus comprising:

a cache to provide access to contents of a memory bank (Fig. 2, element 122);

more than two global buses to provide parallel access to said cache and the memory bank (Fig. 1, multiple buses are disclosed (elements 108, 110, 112, etc)); and

a cache controller to maintain a content of the memory bank in said cache (Fig. 2, element 150 depicts control logic which controls the cache (col. 7, lines 33-41)).

Despite his teachings, Saulsbury fails to disclose providing parallel access of the cache and bank to respond to a request independent of the refresh latency. Leung however discloses an apparatus and a method for hiding the refresh of a memory and providing parallel access of said cache and the memory bank to respond to a request for an access of the memory bank substantially independent of a latency to refresh the memory bank. For instance, in col. 2, lines 34-37, Leung teaches memory banks in parallel with a buffer, each bank independently controlled such that

refresh operations of the banks can be controlled independently. Leung further

discloses performing the refresh operating without delaying external access to the

device in lines 63-65 of col. 2. Additionally Leung teaches the refresh operation as

occurring within the banks when a cache hit occurs – col. 3, lines 7-11.

It would have been obvious to one of ordinary skill in the art at the time of the

invention for Saulsbury to incorporate Leung's apparatus for hiding the refresh of a

memory into his own apparatus. By doing so, Saulsbury's processor/memory device

would benefit by permitting his DRAM device refresh to be completely transparent to

his CPU (i.e. external to the memory) – Leung, col. 2, lines 11-20. Making the refresh

transparent would in turn minimize the system's consumption of memory bandwidth

(Leung col. 1, lines 28-36).

As for claims 16 and 19, Saulsbury teaches a system, comprising:

a core/processor (CPU, Fig 1, element 102); and

a first cache/memory coupled to the core/processor (Fig. 2, element

122), said first cache/memory comprising a second cache to provide access to

contents of a memory bank (Fig. 2 depicts a cache (122) comprising several banks (i.e.

cache storage, buffers, etc.));

more than two global buses to provide parallel access to the

second cache and the memory bank (Fig. 1, multiple buses are disclosed (elements

108, 110, 112, etc));

a cache controller to maintain a content of the memory bank in the

second cache via parallel access of the second cache and the memory bank to

respond to a request for an access of the memory bank substantially independent of a

latency to refresh the memory bank (Fig. 2, element 150 depicts control logic which

controls the cache (col. 7, lines 33-41)).

Despite his teachings, Saulsbury fails to disclose providing parallel access of the

cache and bank to respond to a request independent of the refresh latency.

Leung however discloses an apparatus and a method for hiding the refresh of a

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refresh operations of the banks can be controlled independently. Leung further

discloses performing the refresh operating without delaying external access to the

device in lines 63-65 of col. 2. Additionally Leung teaches the refresh operation as

occurring within the banks when a cache hit occurs – col. 3, lines 7-11.

As for claim 2, Saulsbury teaches the apparatus of claim 1, further

comprising:

a tag buffer coupled to said cache to associate a cache line with a

line of the memory bank (Fig. 2 (element 148) – col. 7, lines 13-20); and

a row decoder coupled to the tag buffer to decode a tag stored in

the tag buffer (Fig. 2 (element 124) – col. 9, lines 43-53 – the decoder is coupled to the

tag buffer via the control logic (150)).

As for claim 3, Saulsbury teaches the apparatus of claim 1, further comprising a dirty bit buffer coupled to the cache to indicate a relationship between a line of the cache and a line of the memory bank (col. 7, lines 13-20 – Fig. 2, element 148). Saulsbury however fails to teach the read access as occurring on a second global bus (different from the first bus used for write access as claimed by applicant). Saulsbury's teachings are limited to using the same bus (Fig. 2, element 116) for read/write control.

Leung however teaches turning off read access to the cache for a first global bus during a cycle and turning on write access to the cache for a second global bus during the cycle after turning off read access (Fig. 1 depicts dedicated read and write global buses DB and DA respectively. Further if a cache miss occurs (i.e. read operation determines that the requested data is not present), the read operation completes and a write operation is initiated in order write back to the cache – col. 3, lines 40-45).

As for claim 4, Saulsbury teaches the apparatus of claim 1, wherein the memory bank comprises dynamic random access memory (Col. 3, lines 35-37 – DRAM).

As for claim 5, Saulsbury teaches the apparatus of claim 1, wherein said cache comprises at least part of a second memory bank (Fig. 2 depicts a cache (122) comprising several banks (i.e. cache storage, buffers, etc.)).

As for claims 6 and 17, Saulsbury teaches the apparatus of claim 1 (and system of claim 17), wherein said more than two global buses comprises two pair of

global buses coupled to the memory bank and said cache (Fig. 1 depicts two data

buses (elements 108 and 110), and two instruction buses (elements 112 and 114)).

As for claims 7, 8, 18 and 20, Saulsbury teaches the apparatus of claim 1

(and system of claims 16 and 20), wherein said cache controller comprises circuitry to

read from (and write to) the memory bank and from (and write to) said cache

substantially simultaneously (Col. 7, lines 33-41, each cache bank is controlled by the

bank logic (element 150). Further, both the cache bank and memory bank are written

to or read from simultaneously at a location specified by the issued data address – col.

9, lines 4-9). Leung too teaches this limitation in col. 7, lines 33-41. Each cache bank

is controlled by the bank logic (element 150). Further, both the cache bank and

memory bank are written to or read from simultaneously at a location specified by the

issued data address – col. 9, lines 4-9.

Conclusion

8.   The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.

Burns et al. (US Patent 6,134,624) teaches a high bandwidth cache

system, which splits read and write access between two global buses (Fig. 6, elements

206 and 210 – Col. 9, lines 7-15). Burns' disclosure further describes motivation for

Saulsbury to split his single control (read/write) bus into separate buses to improve

memory data rate of the system.

9.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.
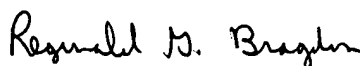
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
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CEW

REGINALD G. BRAGDON
PRIMARY EXAMINER